In the Claims

The following pending claims, claims 1, 2 and 4-18, are presented for the Examiner's convenience:

1. (Amended) A method for manufacturing a wafer-interposer assembly comprising the steps of:

providing a semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads;

providing an interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, and at least one of the second electrical contact pads electrically connected to the one or more communication interfaces;

forming the wafer-interposer assembly by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element; and

singulating the wafer-interposer assembly into one or more chip assemblies.

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2. The method as recited in claim 1, further comprising the steps of:

attaching the wafer-interposer assembly to a testing apparatus; and

testing the semiconductor die.

Please cancel, without prejudice or disclaimer, claim 3.

4. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises performing a parametric test of at least one of the semiconductor die.

5. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises testing the semiconductor die in sequence.

6. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises testing the semiconductor die simultaneously.

7. The method as recited in claim 1 wherein the step of testing the semiconductor chips further comprises using a multiplexer.

8. The method as recited in claim 1 further comprising the step of grading each of the semiconductor die during testing and sorting the semiconductor chips based upon performance level.

9. The method as recited in claim 1 further comprising the step of grading each of the semiconductor die during testing and sorting the semiconductor die into conforming and nonconforming groups.

10. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more integral edge connectors with pins and/or sockets.

11. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more integral bayonet connectors with pins and/or sockets.

12. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more connectors added to the wafer-interposer assembly.

13. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more soldered connections.

14. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more ribbon connectors.

15. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more RF connectors.

16. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more optical or infrared connectors.

17. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more transmit/receive antennas.

18. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more clamps or quick release device.

Remarks

The Examiner has rejected claims 1, 2 and 10-12 under 35 U.S.C. §102(b) as being anticipated by King et al., U.S. Patent No. 5,440,241, (hereinafter "King"). The Examiner has rejected claims 1, 2 and 10-12 under 35 U.S.C. §102(b) as being anticipated by Elder et al., U.S. Patent No. 5,123,850, (hereinafter "Elder").